3. A method of manufacturing a super-junction semiconductor device comprising, in order:

(a) depositing, on a low-resistivity semiconductor substrate of a first conductivity type, at least an epitaxial layer of the first conductivity type which is to become a drift layer;

(b) forming base regions of a second conductivity type and source regions of the first conductivity type, both of which extend to right under end portions of an insulating film mask formed on the epitaxial layer of the first conductivity type by performing selective ion implantation through openings of the insulating film mask and causing thermal diffusion to form planar MOS gate structures in an active portion where a main current is to flow;

(c) forming, by anisotropic etching, using the insulating film mask, trenches that penetrate through the at least one base region and reach the low-resistivity semiconductor substrate or its vicinity;

(d) burying epitaxial layers of the second conductivity type in the respective trenches;

(e) making surfaces of the epitaxial layers of the second conductivity type buried in the trenches approximately flush with a surface of the epitaxial layer of the first conductivity type;

(f) forming regions of the second conductivity type having a higher impurity concentration than the epitaxial layers of the second conductivity type as surface layers of the latter at the same depth as the base regions;

(g) forming high-impurity-concentration regions of the first conductivity type in a prescribed pattern as surface layers of the high-impurity-concentration regions of the other conductivity type at the same depth as the source regions; and

(h) removing the insulating film mask, forming a field oxide film on a peripheral voltage withstanding structure that surrounds the active portion, and then forming prescribed planar MOS gate structures.

4. The method according to claim 3, wherein the field oxide film is a CVD oxide film.

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